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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/784,756	02/23/2004	John McKenna Brennan	5-84-2-6	2203

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EXAMINER	
PAREKH, NITIN	
ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 10/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/784,756	BRENNAN ET AL.	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 12-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 12-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02-23-04* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-10, 12 and 14-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Joshi et al. (US Pat. 5955781)

Regarding claims 1-5, 10 and 12, Joshi et al. disclose a semiconductor device (see Fig. 3) and a method/steps of making such device comprising:

- a semiconductor/silicon substrate (106 in Fig. 3)
- an active region formed in the substrate proximate an upper surface of the substrate (see device/gate-junctions region in Fig. 3), the active region including at least one circuit element formed therein
- a plurality of trenches/channels (108 in Fig. 3) formed in a back surface of the substrate opposite the upper surface of the substrate, the trenches /channels being formed proximate the active region
- the trenches/channels being substantially planar with the back surface of the substrate, and

- wherein the trenches/channels are filled with a thermally conductive material/TCM (see 102 in Fig. 3) such as diamond, the TCM having a thermal conductivity (TC) being greater than that of the substrate (see Table 1) and being configured so as to provide a thermal conduction path for conducting heat away from the active region (Col. 5, line 60- Col. 6, line 5)

(Fig. 3; Col. 4, line 15- Col. 6, line 5; Col. 1-8).

Joshi et al. further teach the trenches/channels having the TCM being formed in the selected regions or the region adjacent or alongside/lengthwise the active regions of the device (Col. 7, lines 5-9; Col. 8, line 26), but fail to:

- explicitly teach the channel being formed substantially entirely through a length of the device between opposing sides of the device and also being formed to reduce a possibility of damage resulting at least in part from a mismatch in coefficients of thermal expansion between a material forming the semiconductor substrate and the thermally conductive material.

The determination of parameters such as size/dimension including length/width, height, thickness, spacing, etc. of the active region/source-gate-drain, metal interconnect, thermally conductive via/plug/channel, substrate/heat sink/thermally conductive structure, etc. in chip packaging and interconnect technology is a subject of

routine experimentation and optimization to achieve the desired thermal/electrical performance, speed, reliability and yield.

Joshi et al further teach using TCM including metals such as tungsten, copper, aluminum, etc. (see Col. 6, lines 43-47; Col. 7, lines 25-27) to provide improved heat dissipation for the device. The metal such as tungsten having a coefficient of thermal expansion (CTE) substantially matching to that of the substrate (see Table 1) provides further protection against any damage due to TCE mismatch between the substrate and the TCM for the thermally conductive channel formed substantially entirely through a length of the device .

It would have been obvious to a person of ordinary skill in the art at the time invention was made to select the channel being formed substantially entirely through a length of the device between opposing sides of the device and also being formed to reduce a possibility of damage resulting at least in part from a mismatch in coefficients of thermal expansion between a material forming the semiconductor substrate and the thermally conductive material so that the thermal dissipation can be improved and the thermal stress and associated defects can be reduced in Joshi et al's device.

Regarding claims 6- 9, Joshi et al. disclose the entire structure as applied to claim 1 above, wherein Joshi et al. further teach:

- the trenches/channels comprising substantially v-shaped grooves having sloped sidewalls (see Fig. 2C; Col. 5, lines 25-52), and

- the trenches/channels being formed using an etching process comprising anisotropic etching (Col. 5, line 65; Col. 6, line52; Col. 8, lines 25-28).

Regarding claim 14, Joshi et al. disclose the entire structure as applied to claim 1 above, wherein Joshi et al. further teach the device structure comprising a plurality of active devices/regions being formed in the upper surface of the substrate such that each of the trenches/channels are proximate a corresponding one of the active devices/regions to provide the desired heat dissipation for the structure (Col. 2, lines 60-65).

Regarding claims 15 and 16, Joshi et al. teach the entire structure as applied to claim 1 above, wherein Joshi et al. further teach the trench/channel being approximately 2-10 microns from a surface of the substrate (see Fig. 2C), but fail to teach at least one channel being formed having a maximum height that is about two thousandths of an inch from the upper surface of the substrate or about forty micrometers from the active region.

The determination of parameters such as size/dimension including length/width, height, spacing, etc. of the active region/source-gate-drain, metal interconnect, thermally conductive via/plug, substrate/ thickness, etc. in chip packaging and interconnect technology is a subject of routine experimentation and optimization to achieve the desired thermal/electrical performance, speed, reliability and yield.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to select at least one channel being formed having a maximum height that is about two thousandths of an inch from the upper surface of the substrate or about forty micrometers from the active region so that the desired thermal dissipation, electrical performance can be achieved and the reliability/yield can be improved in Joshi et al's device.

Regarding claims 17-19, Joshi et al. disclose the steps/method of forming the device as applied to claim 1 above.

Regarding claim 20, Joshi et al. disclose the entire structure as applied to claim 1 above, wherein Joshi et al. further teach the device structure comprising a cooling tower/base (120 in Fig. 5) wherein an integrated circuit die/chip (122 in Fig. 5) is attached to the base to provide a thermal conduction path between the active region and the base for conducting heat away from the active region (Fig. 3 and 5; Col. 6, lines 16-25).

3. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Joshi et al. (US Pat. 5955781) in view of the admitted prior art (APA).

Regarding claims 13, Joshi et al. teach the entire structure as applied to claim 1 above, except the device having a cross-sectional thickness greater than or equal to about six thousandths of an inch.

The APA teaches devices having six mils or more (specification pp. 1)

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the device having a cross-sectional thickness greater than or equal to about six thousandths of an inch as taught by the APA so that warpage can be reduced in Joshi et al's device.

Response to Arguments

4. Applicant's arguments filed on 08-19-05 have been fully considered but they are not persuasive.

A. Applicant contends that there is no motivation to reduce damage to the device/die resulting from a mismatch in coefficients of thermal expansion between the substrate and the thermally conductive material.

However, as explained in the rejections above, Joshi et al. teach using the TCM such as tungsten having the CTE substantially matching to that of the substrate (see Table 1). One of ordinary skill in the art would realize that such TCM would provide the protection against the thermal stress and any damage due to TCE mismatch between the substrate and the TCM.

B. Applicant contends that Joshi et al. teach the etching of BOX layer and not the anisotropic etching of the substrate.

However, Joshi et al. teach etching the trenches/channels in the oxide/BOX layer or in the substrate as required (Col. 5, lines 45-50; Col. 8, lines 25-28). Furthermore, the etching can be accomplished using anisotropic etching (Col. 6, line 52).

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's acting supervisor, Steven Loke can be reached on 571-272-1657.
The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAN or Public PAG. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAG system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Nitin Parekh

NP

NITIN PAREKH

10-19-05

PRIMARY EXAMINER

TECHNOLOGY CENTER 2800